REMARKS

Applicants respectfully traverse and request reconsideration.

As a preliminary matter, Applicants respectfully submit that the finality of the office action should be withdrawn since claims 3, 5, 11 and 16 do not appear to have been rejected. For example, in paragraph 13 of the final office action in referencing claims 3, 5, 11 and 16, it is admitted that among other things, the references do not teach a feedback delay matching circuit that includes serially coupled multiplexer and buffer stages that are coupled in a way as claimed. Then the same paragraph then refers to claims 19 and 20 but does not appear to address claims 3, 5, 11 and 16. It appears that there may have been a typographical error or other error in attempting to reject the claims. Accordingly, Applicants respectfully request that a new office action be submitted that properly rejects these claims if these claims are to be rejected, otherwise Applicants respectfully submit that the claims be identified as being allowable.

In any event, based on Applicants below comments, the above request may be moot since Applicants respectfully submit that the claims are in condition for allowance as they currently stand.

Claims 1, 2, 4, 6, 8, 9, 10, 13, 14, 15 and 18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Applicants' admitted prior art in view of Foss. As Applicants previously noted, the Foss reference is directed to a delayed lock loop implementation for a clock signal that is employed in a synchronous dynamic random access memory. The office action states that "Foss further teaches that the use of such a clock applying circuit, including the feedback delay matching circuit, can be used...in other synchronous memories, such as DDR SDRAM, substantially as claimed." Applicants respectfully request a showing of such a disclosure in Foss. In fact, in column 4, lines 43-49, Foss describes "other synchronous memories" which include video RAMs, SGRAMs, and SROMs. There is no contemplation of double data rate SDRAMs since these SDRAMs operate in a completely different manner

by employing, among other things, a STROBE signal in addition to a clock signal and require different timing and control circuits to operate. In fact, the clock applying circuit described in Foss is directed to compensating for delays associated with a single clock signal and does not contemplate employing multiple clocking and data control operations.

The office action specifically cites the delay model in Foss as the claimed feedback delay matching array. However, as stated in Foss, the Foss reference utilizes a delay lock loop instead of a phase lock loop used in a SDRAM. (See column 2, lines 48-50.) The Foss reference does not contemplate compensating a clock input and a STROBE input using multiple DLLs nor compensating for delay variations associated with a phase shifted output signal drive buffer located in a variable delay circuit that receives a STROBE signal. For example, as noted in Applicants' specification on page 6, lines 7-12, in one embodiment, the feedback delay matching array includes buffer stages that compensate for delay variations associated with, for example, the phase shifted output signal drive buffer 44 and multiplexing circuit 42 in the STROBE receive path. This is a separate path from the clock path. Moreover, as noted in the preamble, the claim is directed to a signal phase shifting circuit that is operative to shift the phase of a STROBE signal based on a clock signal. Foss does not contemplate any type of multiple clock phase circuit such as a feedback delay matching circuit that is coupled to an output of a phase shifting circuit and a signal phase shifting circuit that also employs a variable delay circuit that receives a STROBE signal as claimed. Applicants respectfully submit that the claims must be read as a whole and that there must be some motivation other than Applicants' own specification to combine selected teachings of different references.

For example, it appears that the circuit of Foss is more closely related to the clock signal period dividing circuit 22 as known in the prior art. Applicants also respectfully point out that Foss teaches that the output 29 from the multiplexer 27 even when a delay model 33

is employed, activates the enable buffer 8 to output information from memory. As such, as described in Foss, the delay model uses "similar elements as the real circuit path taken by the input clock signal" to compensate for delays for the input clock signal. Foss does not contemplate, teach or suggest the additional compensation or even a need to compensate for delays associated with a receive path of the STROBE signal that already employs an additional variable delay circuit. As such, the claims are believed to be in condition for allowance.

As to claim 3, for example, as noted above, this claim requires that the feedback delay matching array compensates for delay variations associated with the phase shifted output signal drive buffer that outputs data based on a STROBE signal associated with the double data rate communication. The cited references do not appear to contemplate or render such a circuit obvious since as noted above neither Applicants' admitted prior art nor Foss appear to contemplate such a feedback delay matching array to compensate for the delay variations in a phase shifted output signal driver that is in a variable delay circuit that receives a STROBE signal. Accordingly, this claim is also believed to be in condition for allowance.

The other dependent claims add additional novel and non-obvious subject matter. For example, as to claims 8, 13 and 18, these claim requires, among other things that the feedback delay matching array includes a plurality of serially coupled multiplexer and buffer stages operatively coupled to the plurality of serially coupled buffers of a phase shift generating circuit. It is alleged that items 25 and 27 in Foss are the plurality of serially coupled multiplexer and buffer stages. However, Applicants respectfully note that the Foss reference as described above does not describe the feedback delay matching circuit and in addition, it does not describe a plurality of serially coupled multiplexer and buffer stages but instead appears to show a single multiplexing stage. Accordingly, these claims are also believed to be in condition for allowance.

As to claim 9, Applicants respectfully reassert the relevant remarks made above with respect to claim 1, and as such this claim is also believed to be in condition for allowance.

As to claim 14, Applicants respectfully reassert the relevant remarks made above with respect to claim 1. Accordingly, this claim is also believed to be in condition for allowance.

Claims 3, 5, 11, 16, 19 and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Applicants admitted prior art in view of Foss and further in view of Allen. As noted above, with respect to claims 3, 5, 11 and 16, the office action does not appear to give reasons why this claim is not allowable since there appears to be a typographical error in the rejection, accordingly Applicants respectfully request the finality of the action be withdrawn and a proper rejection of these claims be provided. In any event, as noted above, claim 3 requires, among other things, that the feedback delay matching array includes a plurality of serially coupled buffer stages that are coupled to compensate for delay variations associated with a phase shifted output signal drive buffer. However, as noted above, there is no compensation for any delay associated with element 8 in Foss. Moreover, Allen is directed to a method and apparatus for verifying a non-chip single phase clocking system. A variable delay clock circuit is provided that generates a plurality of delayed clock signals. Such a system appears to teach away from Applicants' claimed invention which is directed to a signal phase shifting circuit that operates to shift the phase of a STROBE signal based on a clock signal. However, as shown in Allen, a single clock is provided in a variable delay clock circuit that generates a plurality of delayed clock signals from the single clock signal. As such, the claims are believed to be in condition for allowance.

Moreover, although Allen discloses serially coupled multiplexer and buffer stages, these plurality of serially coupled buffer stages do not compensate for delay variations associated with a phase shifted output signal driver as required in the claim. Nor do they appear to be part of a feedback delay matching array that is coupled to an output of a phase

shift generating circuit that produces a feedback control signal as required by the claims. Accordingly, these claims are believed to be in condition for allowance.

As to claims 19 and 20, Allen does not appear to teach specified relationship required by the claims nor that the serially coupled multiplexers and buffers are in a feedback delay matching array that is coupled to an output of a phase shift generating circuit as required by the claims. Accordingly, these claims are also in condition for allowance.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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By: _____
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 N. LaSalle Street
Chicago, Illinois 60601
PHONE: (312) 609-7599
FAX: (312) 609-5005